32.8 70GHz CMOS Harmonic Injection-Locked Divider

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Recently, millimeter-wave wireless communication utilizing the 60GHz band has been studied actively, thanks to the availability of as much as 7GHz of BW in this license-free band. In millimeter-wave wireless communication, the design of the PLL, especially the design of the high-speed frequency divider, is a key issue. Although an injection-locked divider (ILD) is a candidate for millimeter-wave operation [1-4], its narrow locking range is a critical drawback for the realization of reproducible systems. In particular, although the cascade connection of ILDs may be necessary for ultrahigh-frequency operation, it degrades the operation margin considerably. To overcome these issues, the output frequency of an ILD should be sufficiently low that a standard CMOS frequency divider with a wide locking range may operate. In this case, the operating margin can be enhanced even with the ILD by utilizing adaptive capacitor trimming, since the low output frequency of the ILD allows a large *LC* product. For this purpose, a harmonic ILD (HILD) [5-7] that divides by more than two is promising. In this paper, a divide-by-four circuit operating at more than 70GHz is reported with a new MOSFET third-harmonic mixer.

In the conventional V-band HILD fabricated with a GaAs pHEMT MMIC [5], cascode FETs with transmission lines operate as a harmonic mixer as well as an oscillator. The self-oscillating cascode FETs generate the third harmonics as well as the fundamental frequency to improve performance. In this circuit, several transmission lines for the fundamental frequency oscillation and the third-harmonic mixer occupy a large area. In the case of CMOS, on the other hand, since an *LC* oscillator occupies less area than one with transmission lines, a harmonic mixer and an oscillator should be separated to reduce the chip area. Here, the third-harmonic is efficiently generated with a single MOSFET without using transmission lines as described later.

A block diagram of the CMOS HILD is shown in Fig. 32.8.1. A divide-by-four circuit is realized by a negative feedback loop containing a third-harmonic mixer. First, to understand the operation of the third-harmonic mixer, the characteristics of the drain current of an NMOSFET as a function of differential drain-source voltage are shown on the left of Fig. 32.8.2, where V_d and V_s vary from 0 to 1V and from 1 to 0V simultaneously, with V_g fixed at 0.6V. In this case, the average voltages of the drain and source are 0.5V. Since, at V_{ds} = 0V, the gate-source voltage is 0.1V, which is less than the threshold voltage, no drain current flows. This causes strong nonlinear characteristics and generates harmonics effectively. Additionally, as shown in Fig. 32.8.2, since drain current is an odd function of the differential drain-source voltage, only odd harmonics are generated when V_{ds} is driven by a sinusoidal wave. The harmonic characteristics of the drain current as a function of $|V_{ds}|$ are shown on the right of Fig. 32.8.2, where the fundamental, second-harmonic, and third-harmonic amplitudes are shown. It is clearly seen that the third-harmonic current is effectively generated by increasing the amplitude of V_{ds}. It is noted that small second harmonics are also observed and are due to the current from the drain or source to the gate through a gate capacitor. When another sinusoidal signal is applied to the gate, the third harmonic of the product of V_{ds} and V_g appears in the drain current. For the divider circuit, the desired component is extracted from the different harmonics in the drain current by an *LC* resonator. A schematic of the CMOS HILD is shown in Fig. 32.8.3. Although the basic topology is similar to that in [4], the injection transistor $M1$ in Fig. 32.8.3 is utilized as a third-harmonic mixer, which mixes the input and the third-harmonic of V_{ds}. To generate nonlinear characteristics, the gate of $M1$ is biased in subthreshold, while the gate of the input transistor in [4] is biased above threshold to obtain sufficient modulation current. The MOS varactor in Fig. 32.8.3 is utilized to increase the lock range, since the output frequency is lower than that in [4], which allows a large *LC* product.

A chip micrograph of the CMOS HILD is shown in Fig. 32.8.4, where a 90nm CMOS process with six metal layers is used. The core size is 110×130μm². The input sensitivity as a function of input frequency is shown in Fig. 32.8.5, where the power consumption is 2.75mW with a supply voltage of 0.5V. It is shown that the minimum and maximum operating frequencies are 62.9 and 71.6GHz, respectively, and operating frequency continuously changes with the changing control voltage of the varactor. The output phase noise and the input and output waveforms of the CMOS HILD are shown in Fig. 32.8.6 when the input and output frequencies are 70 and 17.5GHz, respectively. It is shown that the input signal generator suppresses the phase noise of the CMOS HILD, operating as a divide-by-four circuit, when the output signal is locked to the input. Finally, locking ranges and power consumptions as a function of the maximum operating frequencies for ILDs are compared in Fig. 32.8.7. It is shown that the CMOS HILD realizes both a higher operating frequency and a larger lock range than previously reported CMOS ILDs. The power consumption is 1/3 that of the state-of-the-art GaAs ILD with a comparable operating frequency.

Acknowledgements:
This study was supported by the strategic information and communications R&D promotion program of the ministry of internal affairs and communications of Japan. The VLSI chip in this study has been fabricated through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporation..

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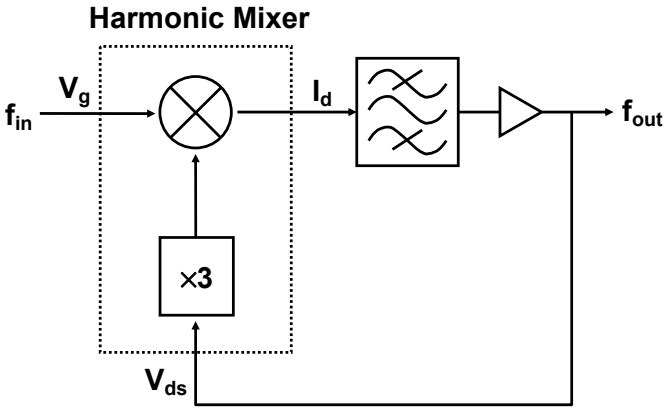

Figure 32.8.1: Block diagram of the harmonic injection-locked divider (HILD).

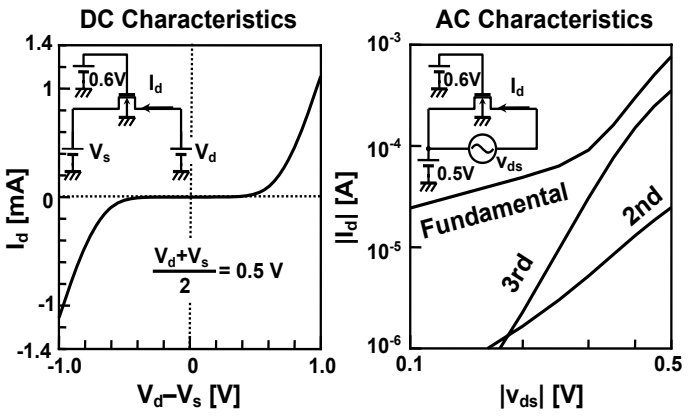

Figure 32.8.2: Simulated drain current of NMOSFET as a function of differential drain-source voltage.

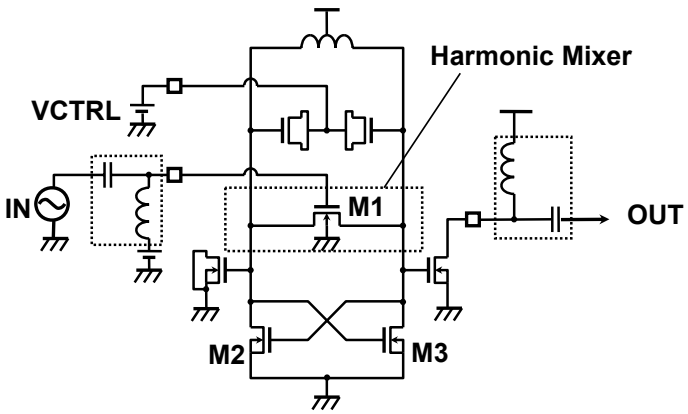

Figure 32.8.3: Schematic diagram of HILD.

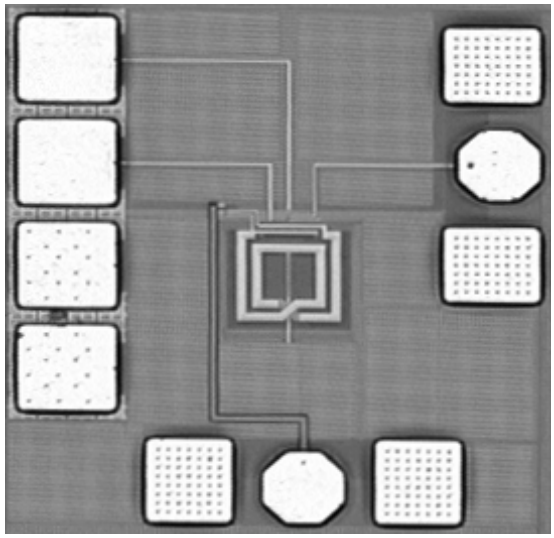

Figure 32.8.4: Chip micrograph of HILD.

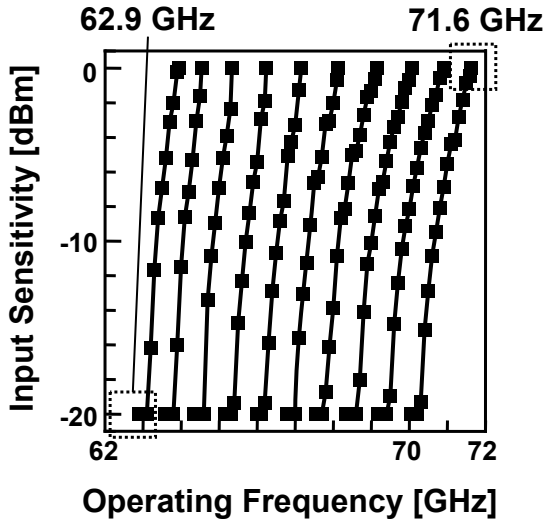

Figure 32.8.5: Measured input sensitivity of HILD.

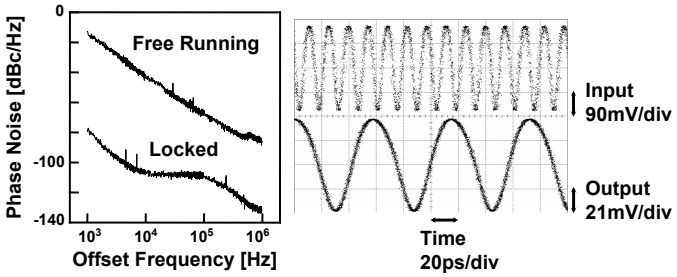

Figure 32.8.6: Measured phase noise and input and output waveforms of HILD when the input and output frequencies are 70 and 17.5GHz, respectively.

Continued on Page 676

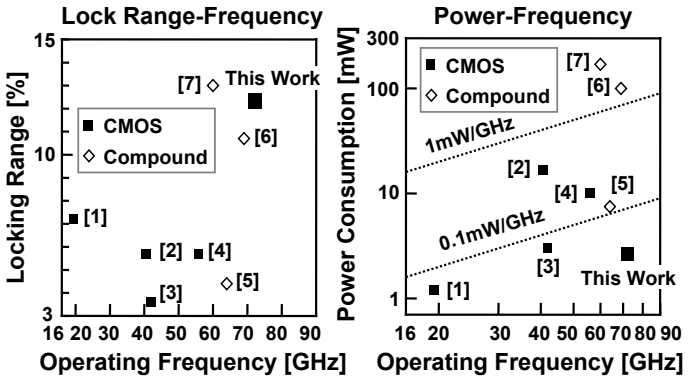

Figure 32.8.7: Comparison of lock ranges and power consumptions as a function of the maximum operating frequencies for injection-lock dividers.

